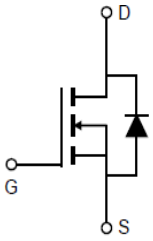
LM3L5N10

100V N-Channel Enhancement Mode MOSFET

Description

The LM3L5N10 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

Inner Equivalent Principium Chart

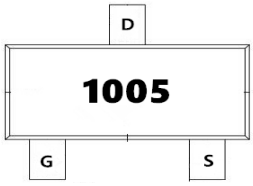


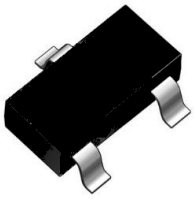
General Features

V_{DS} = 100V I_D =5A

$R_{DS(ON)}$ < 125mΩ @ V_{GS}=10V

Marking and Pin Assignment





Application

Battery protection

Load switch

Uninterruptible power supply

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
LM3L5N10	SOT-23-3	1005	3000

Absolute Maximum Ratings (TC=25℃ unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	5	A
I_D@T_A=70℃	Continuous Drain Current, V_{GS} @ 10V[1]	4.6	A
I_{DM}	Pulsed Drain Current[2]	20	A
P_D@T_A=25℃	Total Power Dissipation[3]	1.5	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
$R_{\theta JA}$	Thermal Resistance Junction-ambient(steady state)[1]	135	℃/W
	Thermal Resistance Junction-ambient(t<10s)[1]	85	℃/W

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100	107	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V,	-	-	1.0	μA
IGSS	Gate to Body Leakage Current	V_{DS}=0V, V_{GS}=±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.0	1.5	2.5	V
RDS(on)	Static Drain-Source on-Resistance note3	V_{GS}=10V, I_D=10A	-	105	125	mΩ
		V_{GS}=4.5V, I_D=8A	-	125	135	mΩ
C_{iss}	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	-	610	-	pF
Coss	Output Capacitance		-	40	-	pF
Crss	Reverse Transfer Capacitance		-	25	-	pF
Q_g	Total Gate Charge	V_{DS}=30V, I_D=10A, V_{GS}=10V	-	12	-	nC
Q_{gs}	Gate-Source Charge		-	2.2	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	2.5	-	nC
td(on)	Turn-on Delay Time	V_{DS}=30V, I_D=5A, R_G=1.8Ω, V_{GS}=10V	-	7	-	ns
t_r	Turn-on Rise Time		-	5	-	ns
td(off)	Turn-off Delay Time		-	16	-	ns
t_f	Turn-off Fall Time		-	6	-	ns
IS	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	-	-	10	A
ISM	Pulsed Source Current[2,5]		-	-	40	A
VSD	Diode Forward Voltage[2]	V_{GS}=0V, I_S=10A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	I_F=10A, dI/dt=100A/μs	-	21	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	21	-	nC

Note :

1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=11A

4.The power dissipation is limited by 150°C junction temperature

5 .The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

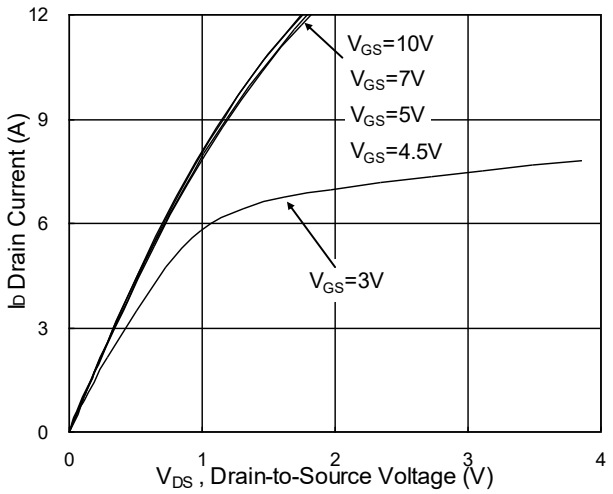


Fig.1 Typical Output Characteristics

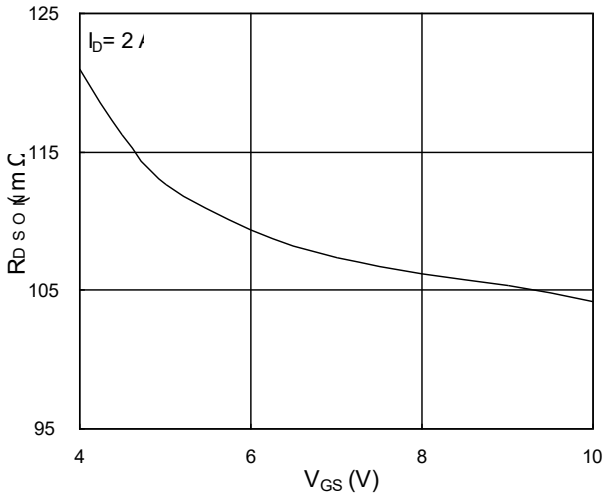


Fig.2 On-Resistance vs. Gate-Source

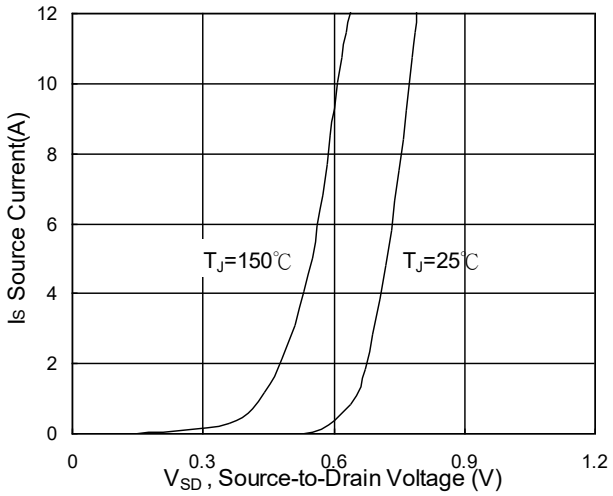


Fig.3 Forward Characteristics Of Reverse

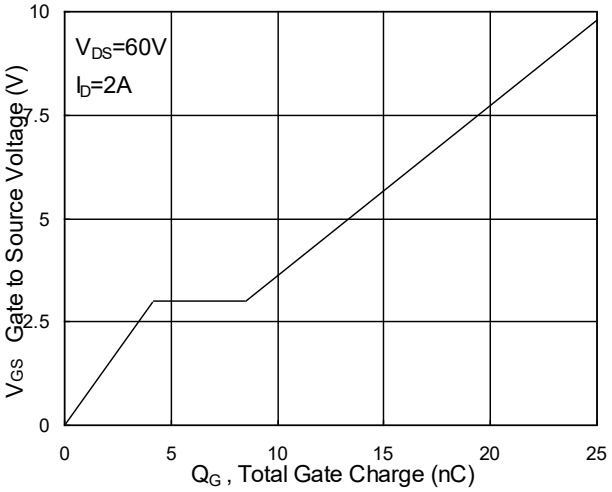


Fig.4 Gate-Charge Characteristics

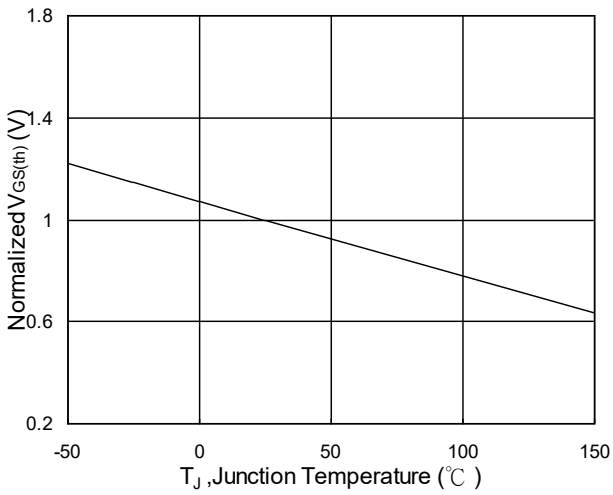


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

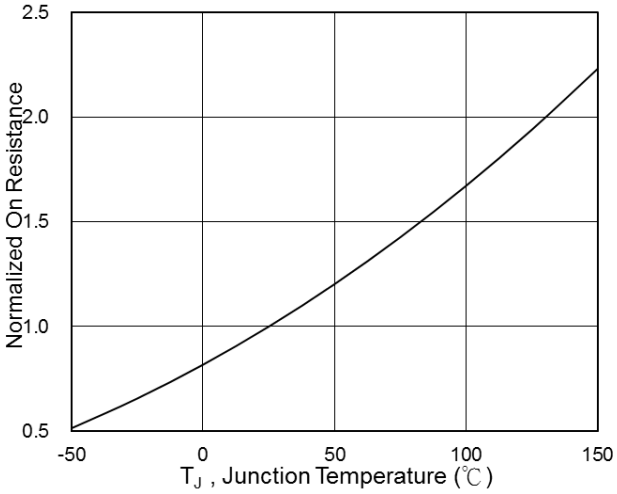


Fig.6 Normalized R_{DSON} vs. T_J

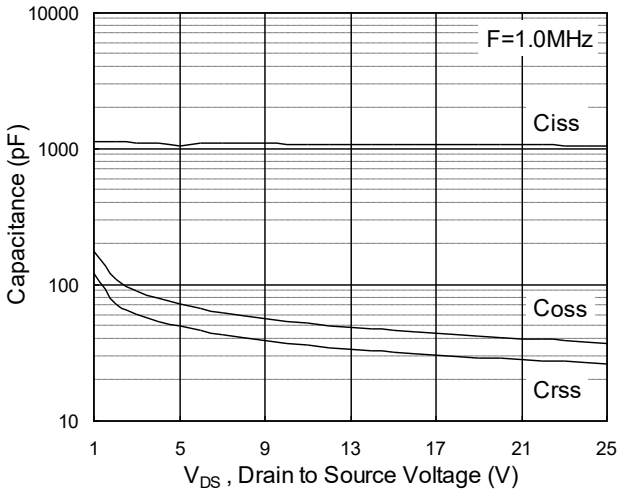


Fig.7 Capacitance

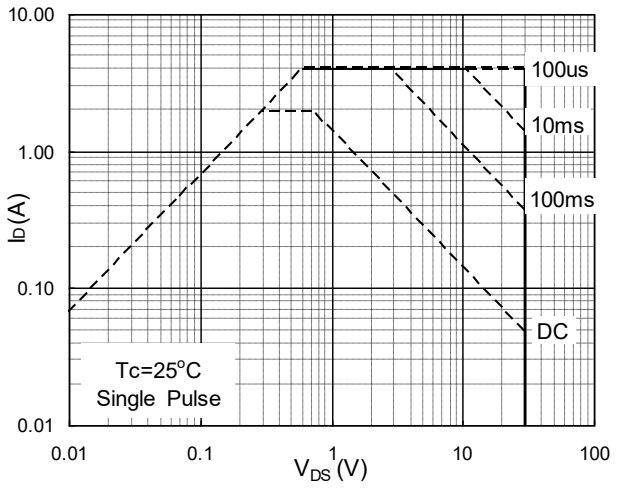


Fig.8 Safe Operating Area

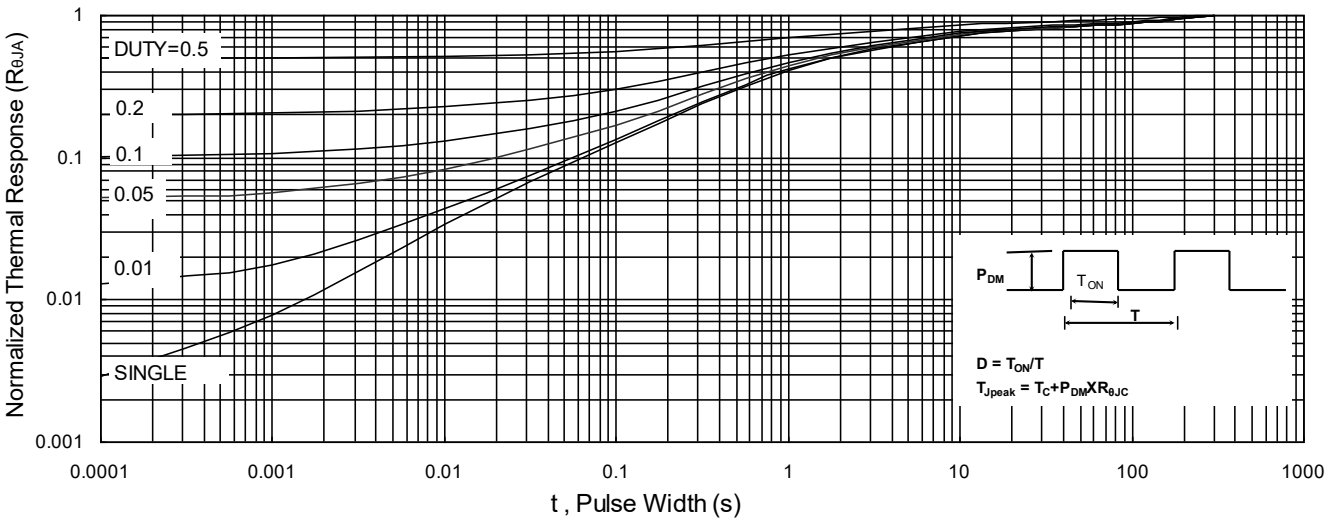


Fig.9 Normalized Maximum Transient Thermal Impedance

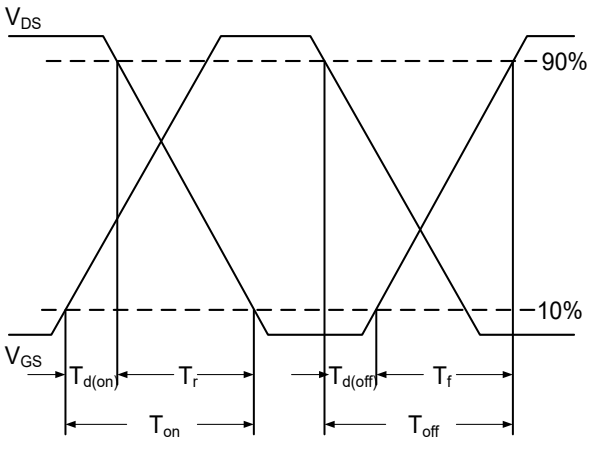


Fig.10 Switching Time Waveform

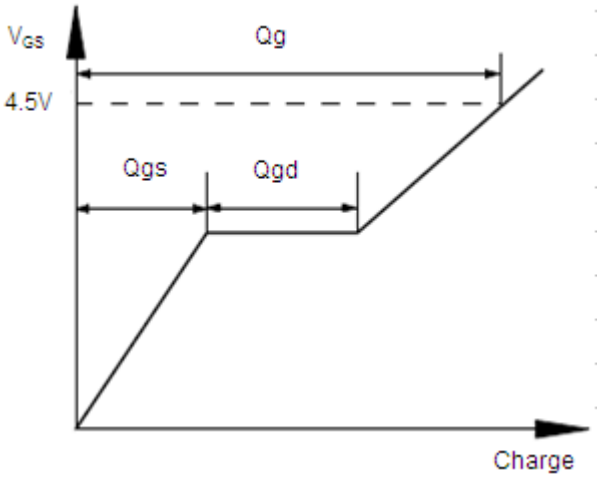
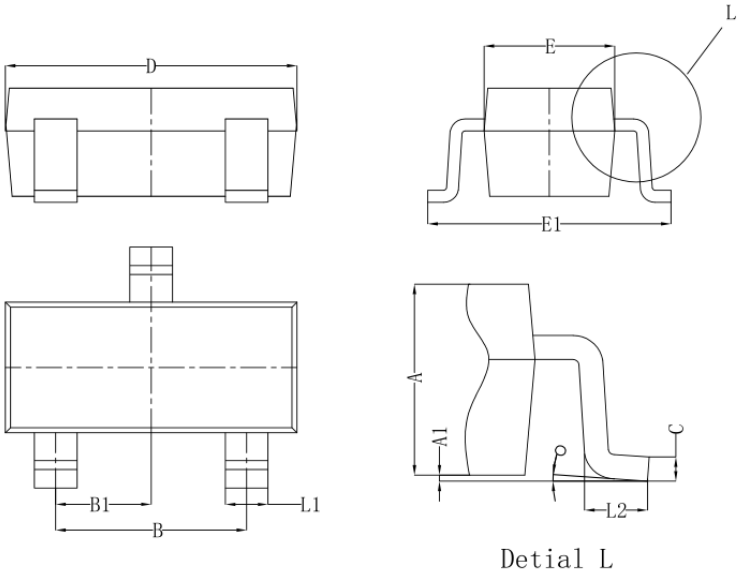


Fig.11 Gate Charge Waveform

Package Outline



Symbol	Dim in mm		
	Min	Nor	Max
A	1.050	1.100	1.150
A1	0.000	0.050	0.100
L1	0.300	0.400	0.500
C	0.100	0.150	0.200
D	2.820	2.920	3.020
E	1.500	1.600	1.700
E1	2.650	2.800	2.950
B	1.800	1.900	2.000
B1	0.950 TYP		
L2	0.300	0.450	0.600
o	0°	4°	8°

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