



General Description

The LM6L3N10 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The LM6L3N10 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

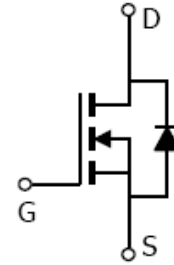
General Features

- $V_{DS} = 100V$ $I_D = 3A$
- $R_{DS(ON)} < 250m\Omega @ V_{GS} = 10V$
- High density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-6L package design

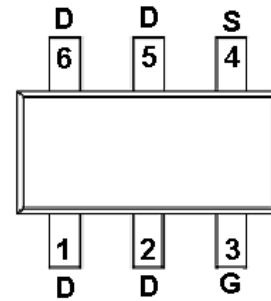
Applications

- Powered System
- DC/DC Converter
- Load Switch

Inner Equivalent Principium Chart



Pin Assignment



Package Marking and Ordering Information

Device	Device Marking	Device Package	Reel Size	Tape width	Quantity
LM6L3N10	M10K/MK	SOT-23-6L	-	-	3000 units

Absolute Maximum Ratings

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V_{DSS}	100	V
Gate -Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current($T_J = 150^\circ C$)	I_D	$T_A = 25^\circ C$	3.0
		$T_A = 70^\circ C$	2.0
Pulsed Drain Current	I_{DM}	10	A
Power Dissipation	P_D	$T_A = 25^\circ C$	1.25
		$T_A = 70^\circ C$	0.8
Operating Junction Temperature	T_J	-55/150	$^\circ C$
Storage Temperature Range	T_{STG}	-55/150	$^\circ C$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	100	$^\circ C/W$

**Electrical Characteristic** ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	2.0	2.5	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$			1	uA
		$V_{DS}=80V, V_{GS}=0V$ $T_J=125^\circ\text{C}$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 5V, V_{GS}=10V$	3.0			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=3A$		0.18	0.25	Ω
Forward Transconductance	g_{fs}	$V_{DS}=10V, I_D=3A$		2.4		S
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$			1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=80V, V_{GS}=10V$ $I_D=5A$		9	13	nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			1.4		
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V$ $f=1\text{MHz}$		508		pF
Output Capacitance	C_{oss}			29		
Reverse Transfer Capacitance	C_{rss}			16.5		
Turn-On Time	$t_{d(on)}$	$V_{DD}=50V, R_L=10\Omega$ $I_D=3A, V_{GEN}=10V$ $R_G=3.3\Omega$		2		nS
	t_r			21.5		
Turn-Off Time	$t_{d(off)}$			11.2		
	t_f			18.8		

Characteristics Curve

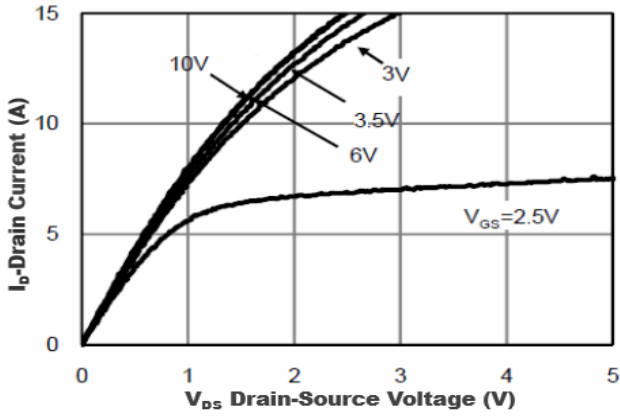


Figure1. Output Characteristics

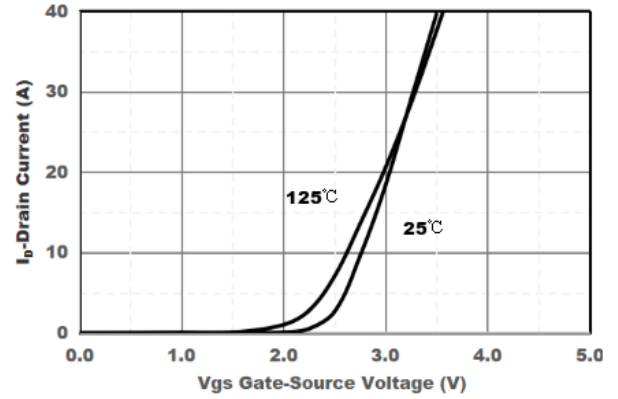


Figure2. Transfer Characteristics

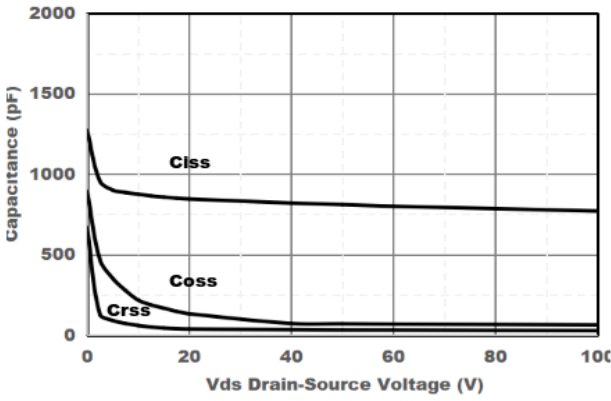


Figure3. Capacitance Characteristics

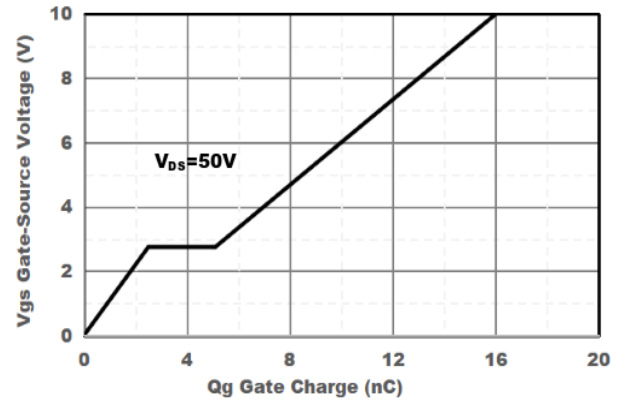


Figure4. Gate Charge

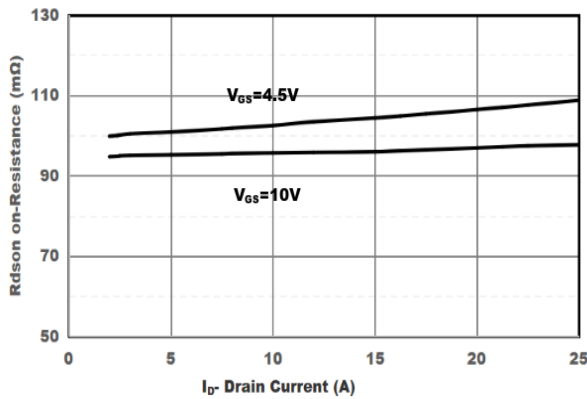


Figure5. Drain-Source on Resistance

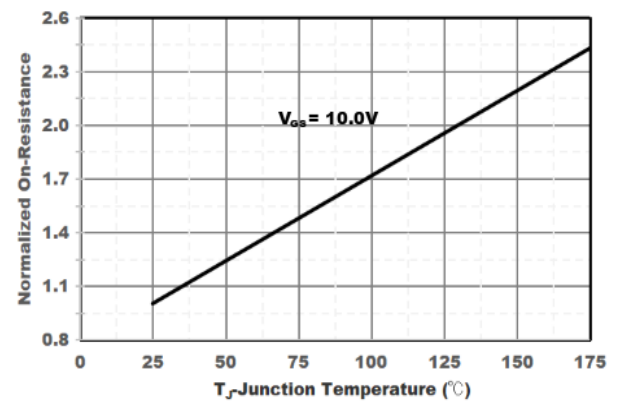


Figure6. Drain-Source on Resistance

Test Circuit & Waveform

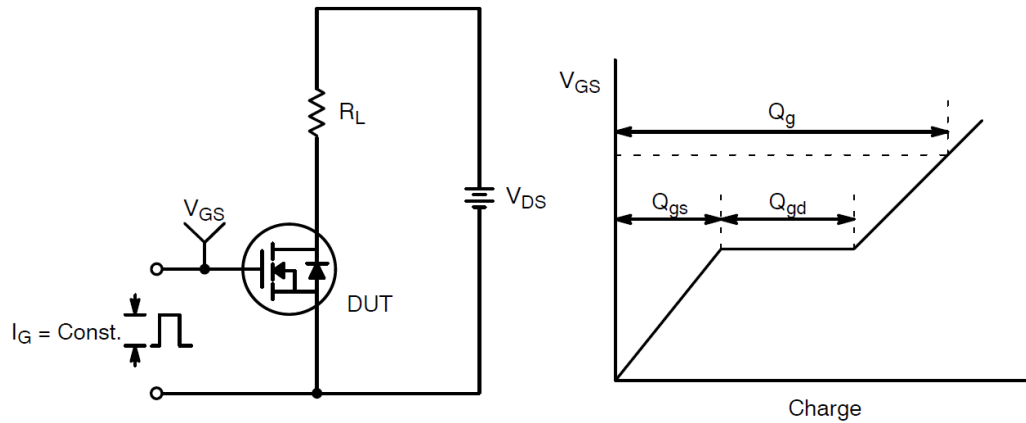


Figure 14: Gate Charge Test Circuit & Waveform

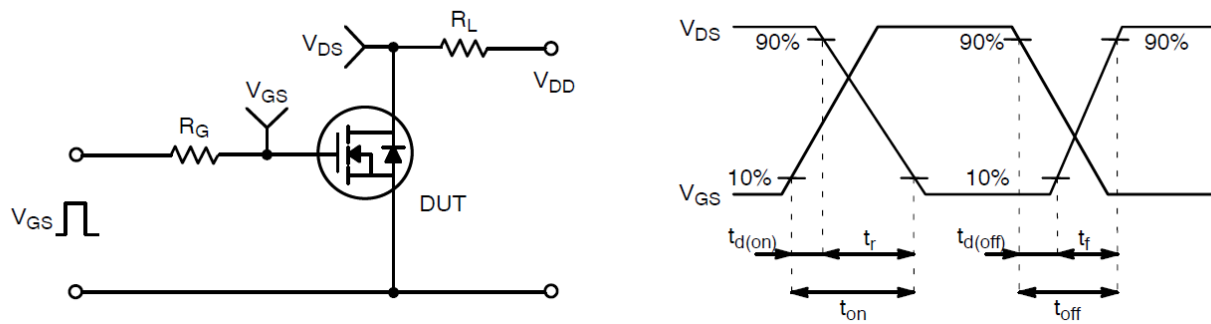


Figure 15: Resistive Switching Test Circuit & Waveforms

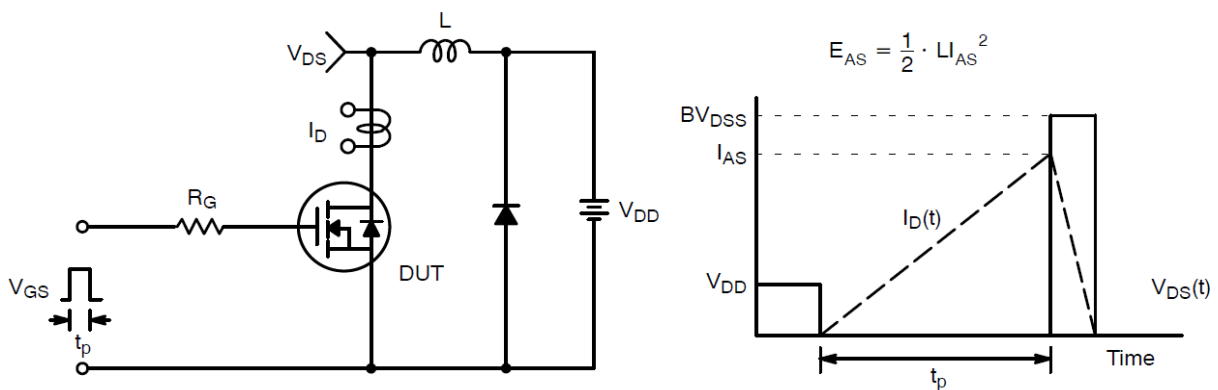
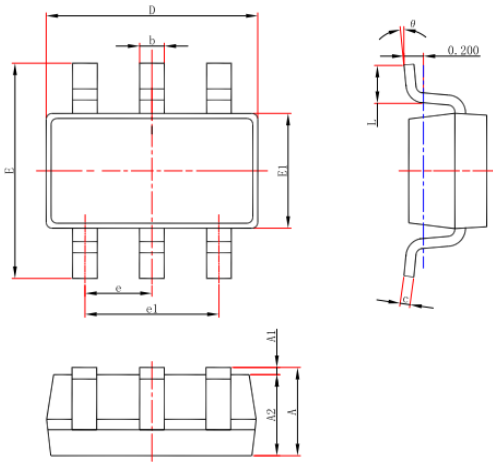


Figure 16: Unclamped Inductive Switching Test Circuit & Waveforms

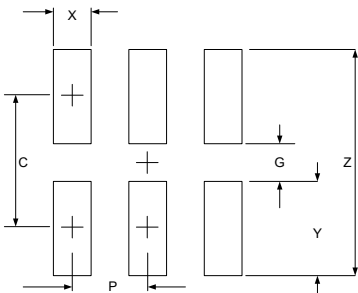


SOT-23-6L Package information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
C	2.50	0.098
G	1.40	0.055
P	0.95	0.037
X	0.60	0.024
Y	1.10	0.043
Z	3.60	0.141

NOTICE

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