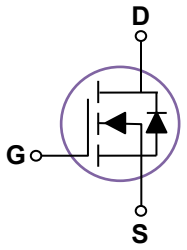
LM10110

100V N-Channel Enhancement Mode MOSFET

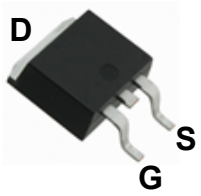
General Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Inner Equivalent Principium Chart



Pin Assignment



General Features

V_{DS} = 100V I_D =15A

$R_{DS(ON)}$ < 110mΩ @ V_{GS} =10V

Package Marking and Ordering Information

Marking	Part Number	Package	Packing	Qty.
10110	LM10110	TO-252	Reel	2500Pcs

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous	TC=25°C	I_D	15	A
	TC=100°C	I_D	10.5	A
Drain Current – Pulsed		I_{DM}	60	A
Maximum Power Dissipation		P_D	34	W
Single pulse avalanche energy(1)		E_{AS}	9	mJ
Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150	℃

Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance junction-case	$R_{\theta Jc}$		2.5	℃ /W
Thermal Resistance unction-to-Ambient	$R_{\theta JA}$		62	℃ /W

Electrical Characteristics (TJ=25℃ unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	100			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V,V_{GS}=0V			1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.2	1.6	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=10A		80	110	mΩ
		V_{GS}=4.5V, I_D=8A		90	125	mΩ
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{DS}=25V,V_{GS}=0V, F=1.0MHz		1200		pF
C_{oss}	Output Capacitance			60		pF
C_{rss}	Reverse Transfer Capacitance			35		pF
SWITCHING PARAMETERS						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=50V,I_D=1A, V_{GS}=10V, R_G=6Ω		18		nS
t_r	Turn-on Rise Time			4		nS
$t_{d(off)}$	Turn-Off Delay Time			40		nS
t_f	Turn-Off Fall Time			3		nS
Q_g	Total Gate Charge	V_{DS}=50V,I_D=2A, V_{GS}=10V		20		nC
Q_{gs}	Gate-Source Charge			3.2		nC
Q_{gd}	Gate-Drain Charge			3.6		nC
Rg	Gate resistance	V_{GS}=0V, V_{DS}=0V, F=1MHz		2		Ω
V_{SD}	Diode Forward Voltage	V_{GS}=0V,I_{SD}=1A		0.7	1.2	V

Note:

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. V_{DD}=50V,V_{GS}=10V,L=0.1mH,IAS=12A., Starting TJ=25℃
3. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
4. Essentially independent of operating temperature.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

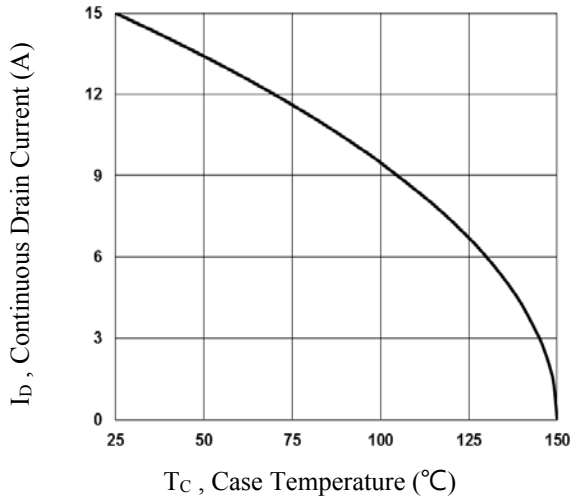


Fig.1 Continuous Drain Current vs. T_C

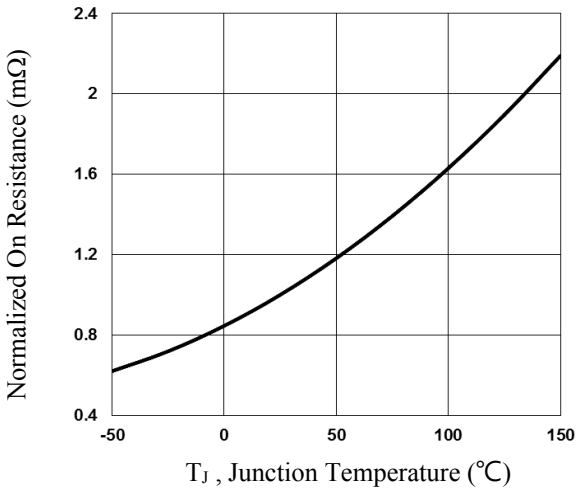


Fig.2 Normalized RDSON vs. T_J

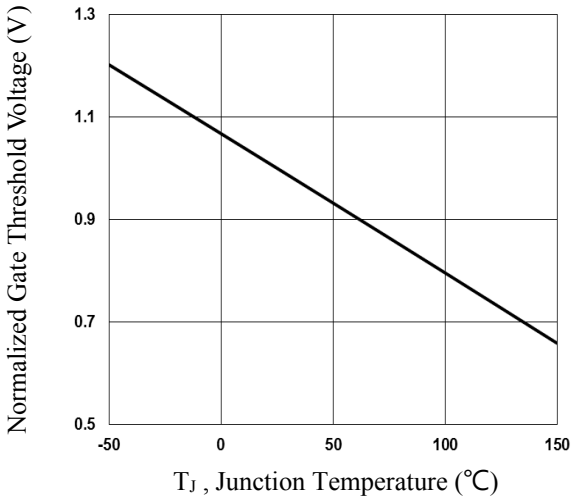


Fig.3 Normalized V_{th} vs. T_J

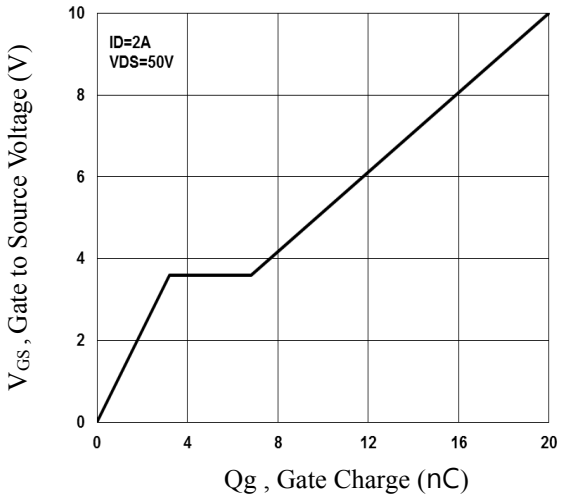


Fig.4 Gate Charge Waveform

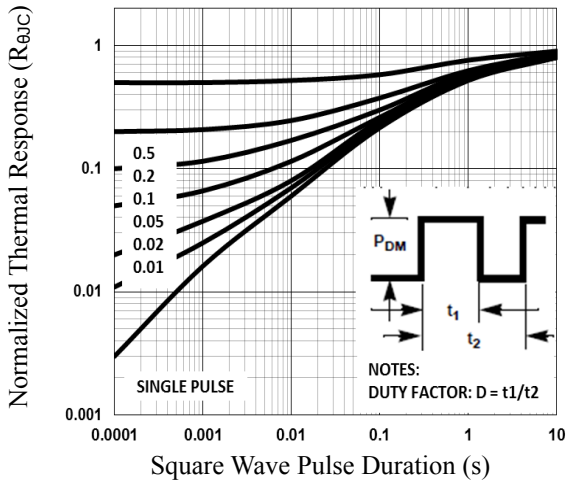


Fig.5 Normalized Transient Impedance

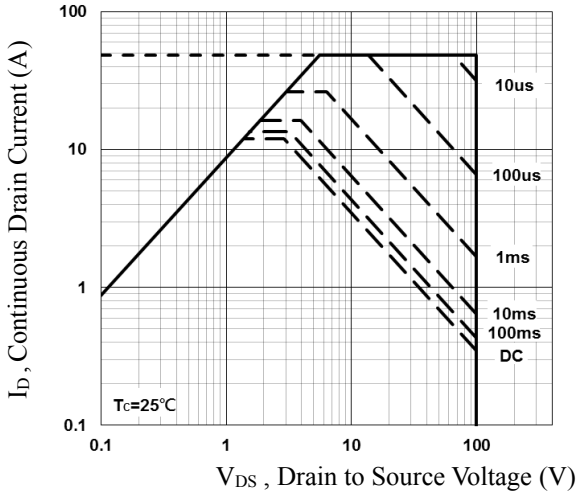


Fig.6 Maximum Safe Operation Area

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

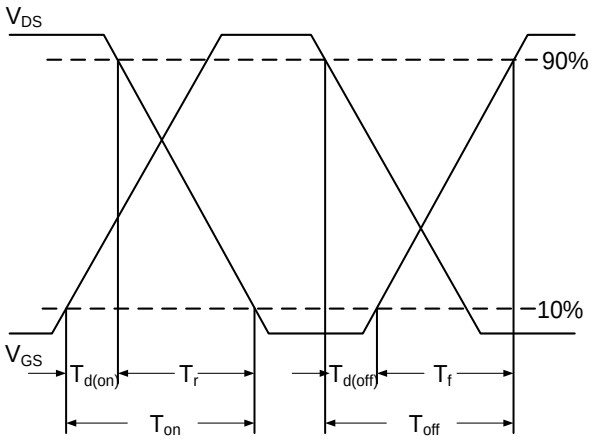


Fig.7 Switching Time Waveform

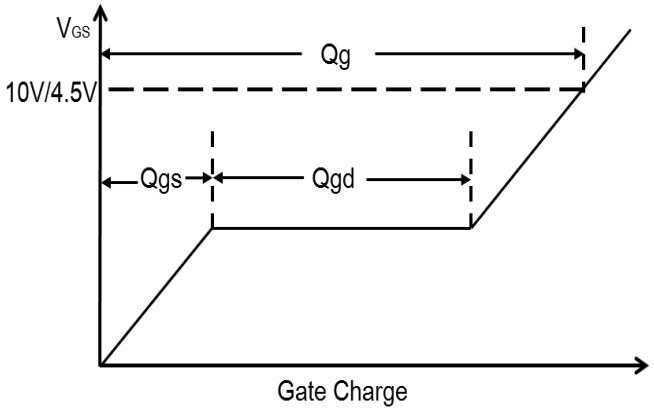
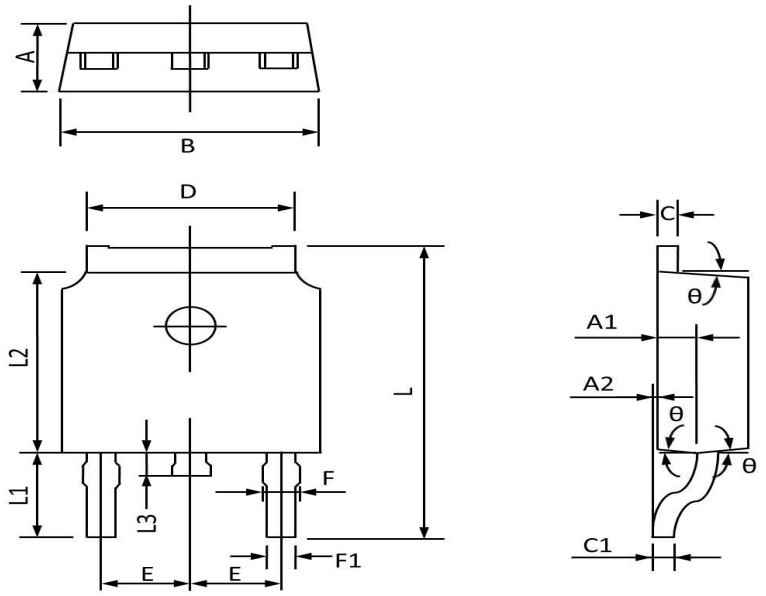


Fig.8 Gate Charge Waveform

Package Outline



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MAX	MIN	MAX	MIN
A	2.400	2.200	0.094	0.087
A1	1.110	0.910	0.044	0.036
A2	0.150	0.000	0.006	0.000
B	6.800	6.400	0.268	0.252
C	0.580	0.450	0.023	0.018
C1	0.580	0.460	0.023	0.018
D	5.500	5.100	0.217	0.201
E	2.386	2.186	0.094	0.086
F	1.140	0.600	0.045	0.024
F1	0.880	0.500	0.035	0.020
L	10.400	9.400	0.409	0.370
L1	3.000	2.400	0.118	0.094
L2	6.223	5.400	0.245	0.213
L3	1.200	0.600	0.047	0.024
θ	9°	3°	9°	3°

Shanghai Leiditech Electronic Co.,Ltd
Email: sale1@leiditech.com
Tel : +86- 021 50828806
Fax : +86- 021 50477059