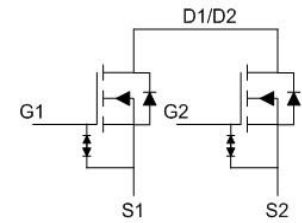


General Description

The LM4D8809 is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent R_{DS(ON)} and gate charge for most of the small power switching and load switch applications. The meet the RoHS and Product requirement with full function reliability approved.



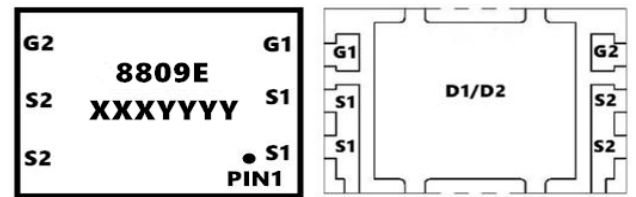
General Features

$V_{DS} = 20V$ $I_D = 9.5A$

$R_{DS(ON)} < 9m\Omega$ @ $V_{GS}=4.5V$

$R_{DS(ON)} < 13.5m\Omega$ @ $V_{GS}=2.5V$

ESD=2KV HBM

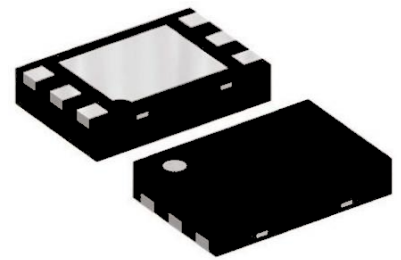


Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
LM4D8809	DFN2*3-6	8809E	3000

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	± 12	V
$I_D@T_A=25^\circ C$	Continuous Drain Current, V_{GS} @ 4.5V ¹	9.5	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, V_{GS} @ 4.5V ¹	7.6	A
I_{DM}	Pulsed Drain Current ²	60	A
$P_D@T_A=25^\circ C$	Total Power Dissipation ¹	1.56	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹ (t ≤ 10s)	80	$^\circ C/W$

N-Channel Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=4.5V, I_D=5A$	6.3	7.8	9	m Ω
		$V_{GS}=4.0V, I_D=5A$	6.5	8.0	9.5	
		$V_{GS}=3.7V, I_D=5A$	6.7	8.2	10	
		$V_{GS}=3.1V, I_D=5A$	7.1	8.7	11.2	
		$V_{GS}=2.5V, I_D=5A$	8.0	10.5	13.5	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	0.45	---	1.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=16V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	---	---	1	μA
		$V_{DS}=16V, V_{GS}=0V, T_J=55^{\circ}\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 12V, V_{DS}=0V$	---	---	± 10	μA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=5.5A$	---	38	---	S
Q_g	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=5.5A$	---	22	---	nC
Q_{gs}	Gate-Source Charge		---	3.1	---	
Q_{gd}	Gate-Drain Charge		---	8.2	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=4.5V, R_G=6, I_D=5.5A$	---	10	---	ns
T_r	Rise Time		---	39.5	---	
$T_{d(off)}$	Turn-Off Delay Time		---	65	---	
T_f	Fall Time		---	30	---	
C_{iss}	Input Capacitance	$V_{DS}=10V, V_{GS}=0V, f=1\text{MHz}$	---	1647	---	pF
C_{oss}	Output Capacitance		---	170	---	
C_{rss}	Reverse Transfer Capacitance		---	148	---	
I_S	Continuous Source Current ¹	$V_G=V_D=0V$, Force Current	---	---	9.5	A
I_{SM}	Pulsed Source Current ²		---	---	60	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=9.5A, T_J=25^{\circ}\text{C}$	---	---	1.2	V

Note :

- 1 .The data tested by surface mounted on a 1 inch²FR-4 board with 2OZ copper, $t \leq 10s$.
- 2.The data tested by pulsed , pulse width $\leq 10\mu s$, duty cycle $\leq 1\%$

Typical Characteristics

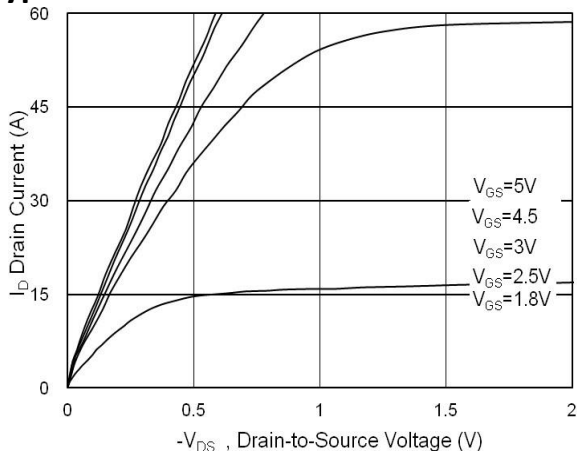


Fig.1 Typical Output Characteristics

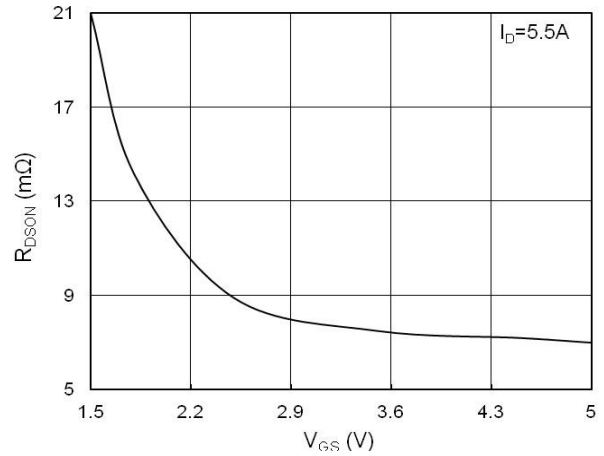


Fig.2 On-Resistance vs. Gate-Source

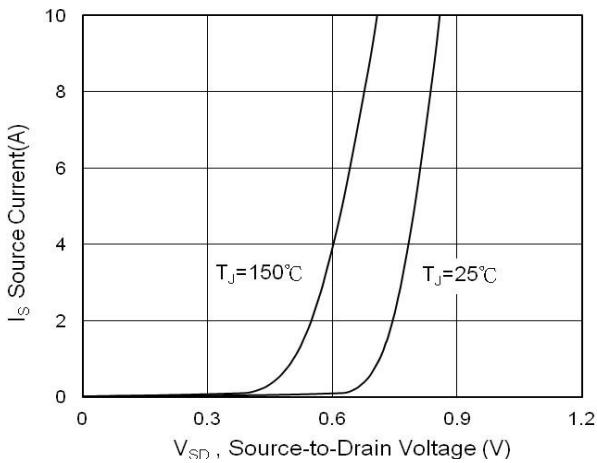


Fig.3 Forward Characteristics Of Reverse

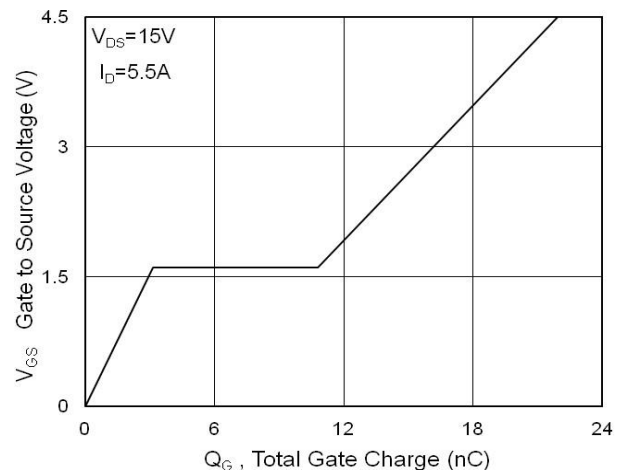


Fig.4 Gate-Charge Characteristics

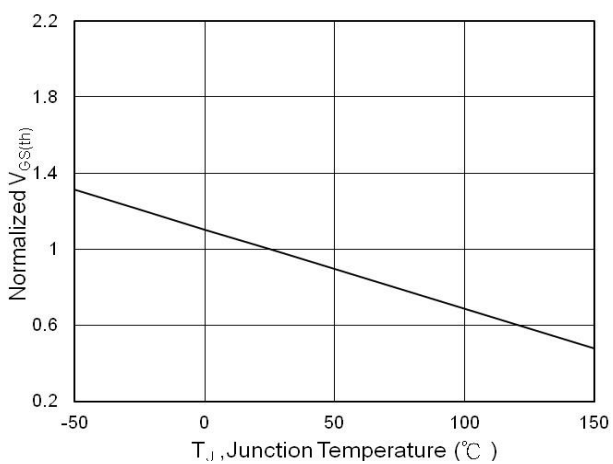


Fig.5 $V_{GS(th)}$ vs. T_J

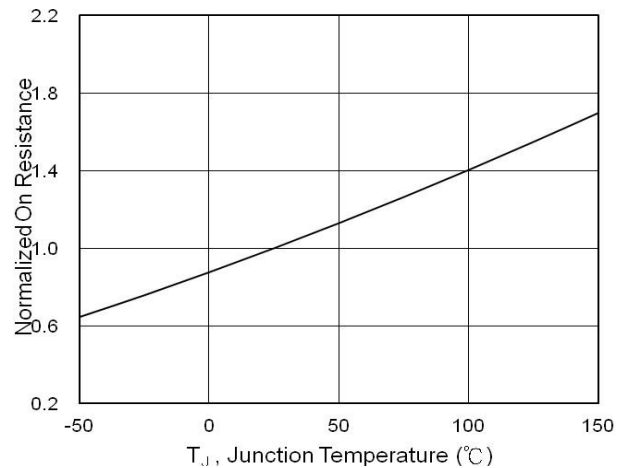


Fig.6 Normalized $R_{DS(ON)}$ vs. T_J

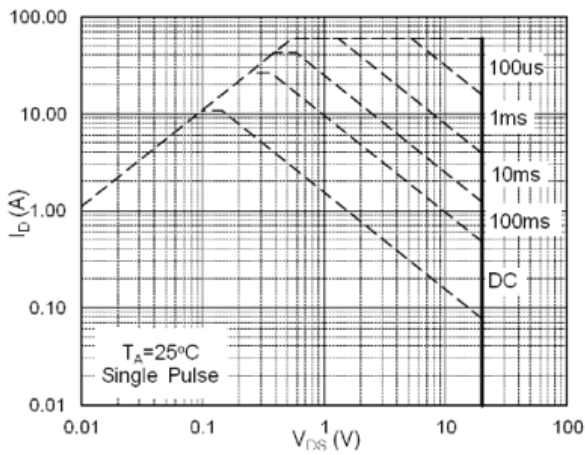


Fig.8 Safe Operating Area

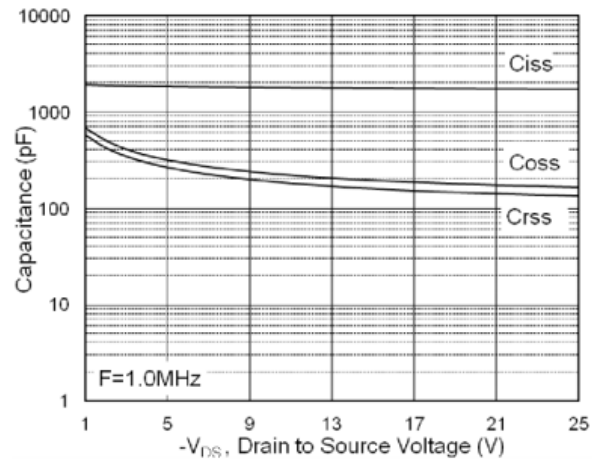


Fig.7 Capacitance

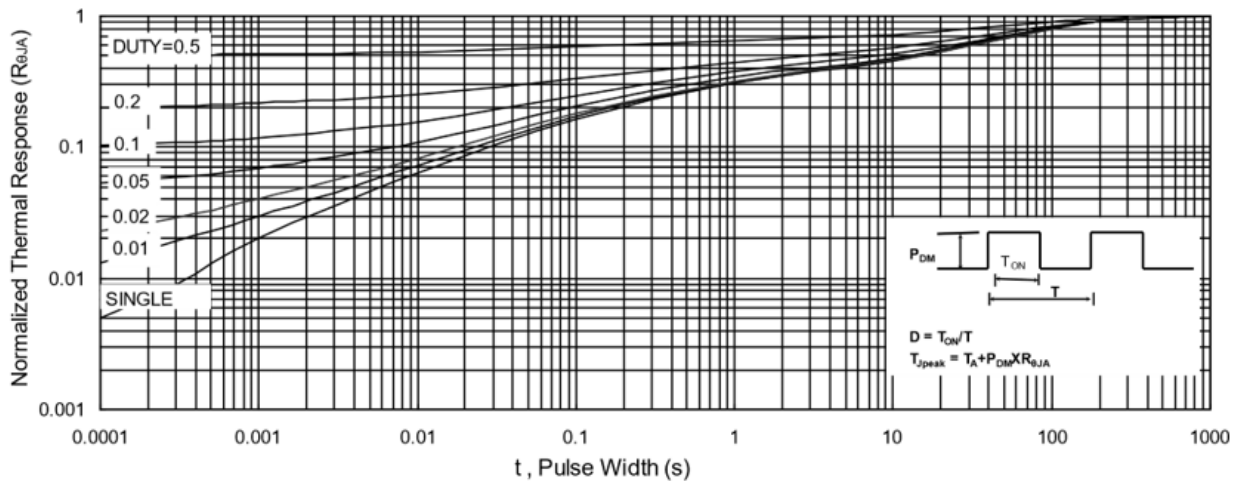


Fig.9 Normalized Maximum Transient Thermal Impedance

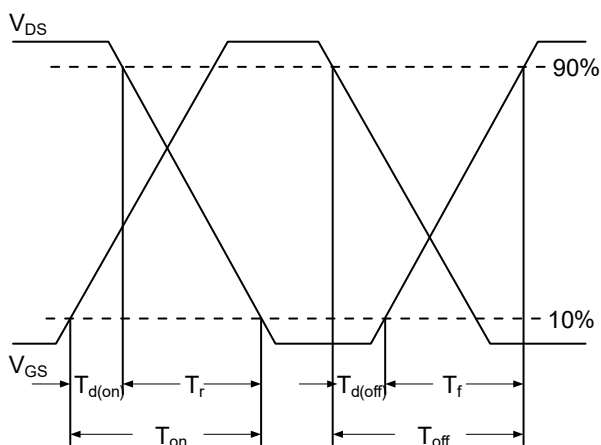


Fig.10 Switching Time Waveform

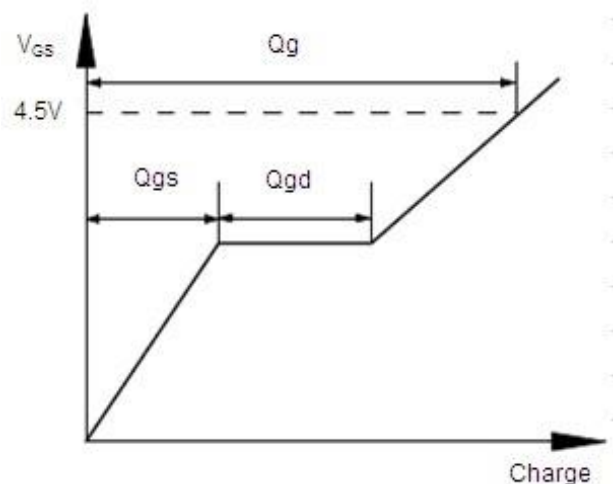
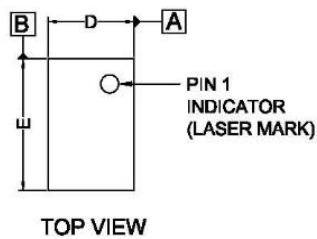
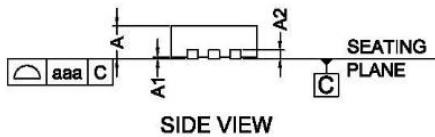
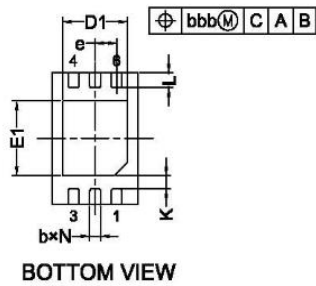


Fig.11 Gate Charge Waveform

PACK DFN2*3-6



COMMON DIMENSIONS (UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.203		
b	0.20	0.25	0.30
D	1.95	2.00	2.05
D1	1.45	1.50	1.55
E	2.95	3.00	3.05
E1	1.65	1.70	1.75
e	0.50BSC		
L	0.30	0.35	0.40
K	0.20MIN		
N	6		
aaa	0.08		
bbb	0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS THE TERMINALS.