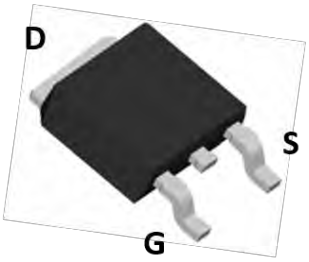
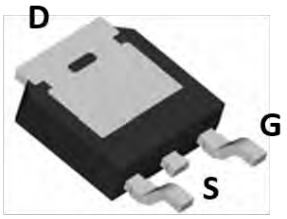
Leiditech

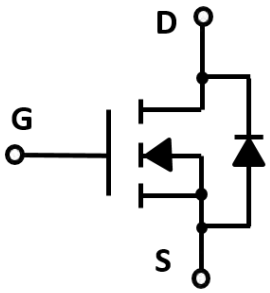
LMD25N15B

N-ChannelEnhancement Mode Field Effect Transistor





TO-252



Product Summary

- V_{DS} 150V
- I_D 25A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜75 mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜88 mohm

General Description

- Split Gate Trench MOSFET technology
- High Speed Power Switching, logic level
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested

Applications

- Synchronous Rectification in SMPS
- Hard Switching and High Speed Circuit
- Power Tools
- UPS
- Motor Control

■ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	150	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_C=25℃	I_D	25	A
	T_C=100℃		16	
Pulsed Drain Current [A]		I_{DM}	90	A
Avalanche Energy, Single Pulse [B]		E_{AS}	3.75	mJ
Total Power Dissipation @ T_C=25℃		P_D	52	W
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	2.4	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
LMD25N15B	F2		2500	2500		13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Static Parameter							
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA		150			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=150V,V_{GS}=0V	T_J=25℃			1	μA
			T_J=100℃			100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V				±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA		1.0	2.0	3.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=5.0A			63	75	mΩ
		V_{GS}=4.5V, I_D=4.0A			70	88	
Trans conductance	g_{fs}	V_{DS} =5V, I_D =15A			18		S
Gate Resistance	R_G	V_{GS} =0V, V_{DS} Open, f=1MHz			5.0		Ω
Diode Forward Voltage	V_{SD}	I_S=15.0A,V_{GS}=0V			0.9	1.2	V
Maximum Body-Diode Continuous Current	I_S					15.0	A
Dynamic Parameters							
Input Capacitance	C_{iss}	V_{DS}=75V,V_{GS}=0V,f=1MHZ			625		pF
Output Capacitance	C_{oss}				37		
Reverse Transfer Capacitance	C_{rss}				13		
Switching Parameters							
Total Gate Charge (10V)	Q_g (10V)	V_{GS}=10V,V_{DD}=75V,I_D=5A			11.6		nC
Total Gate Charge (4.5V)	Q_g (4.5V)				6.5		
Gate Source Charge	Q_{gs}				1.2		
Gate Drain Charge	Q_{gd}				4		
Turn-on Delay Time	$t_{d(on)}$	V_{GS}=10V,V_{DD}=75V, I_D=5A, R_{GEN}=10Ω			10		ns
Turn-on Rise Time	t_r				7		
Turn-off Delay Time	$t_{d(off)}$				14		
Turn-off Fall Time	t_f				3		
Reverse Recovery Time	t_{rr}	V_R =75V, I_F =5A, dI_F/dt=100A/μs			50		ns
Reverse Recovery Charge	Q_{rr}				70		nC

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.
B. L=0.3mH, T_A =25℃.

■ Typical Performance Characteristics

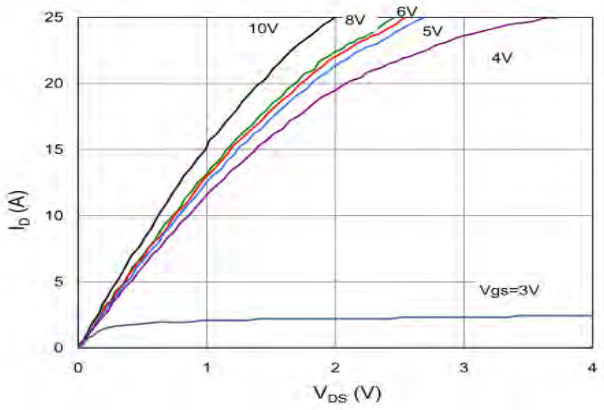


Figure1. Output Characteristics

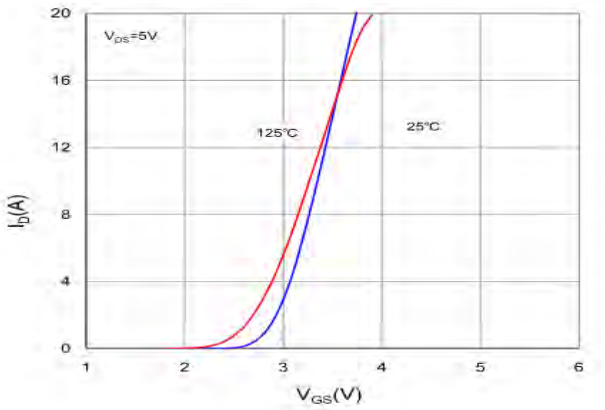


Figure2. Transfer Characteristics

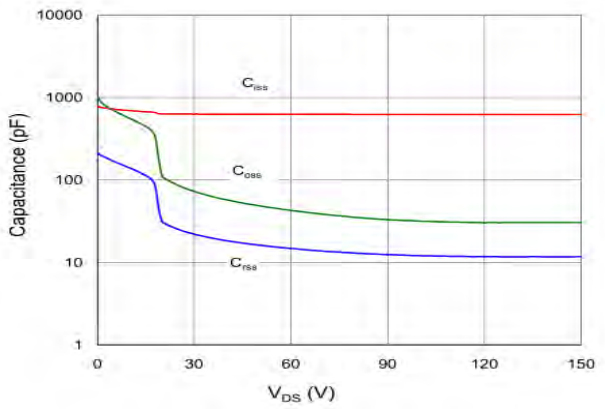


Figure3. Capacitance Characteristics

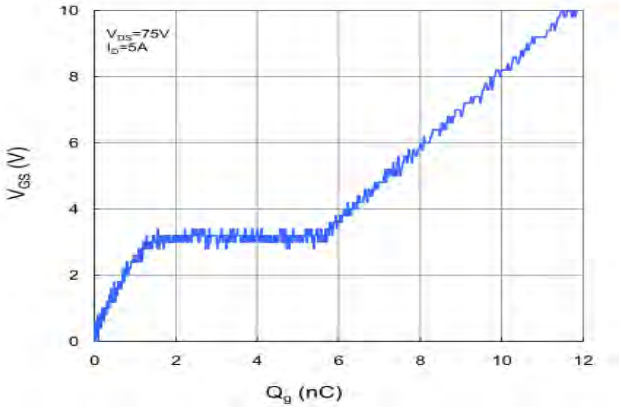


Figure4. Gate Charge

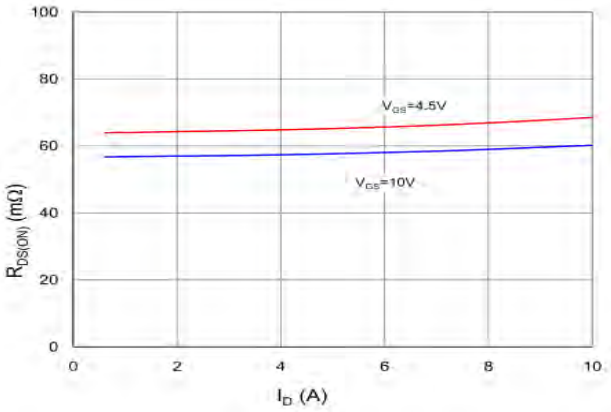


Figure5. Drain-Source on Resistance

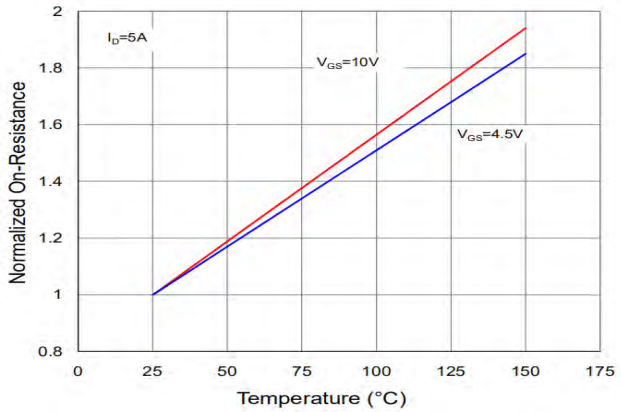


Figure6. Normalized On-Resistance vs. Junction Temperature

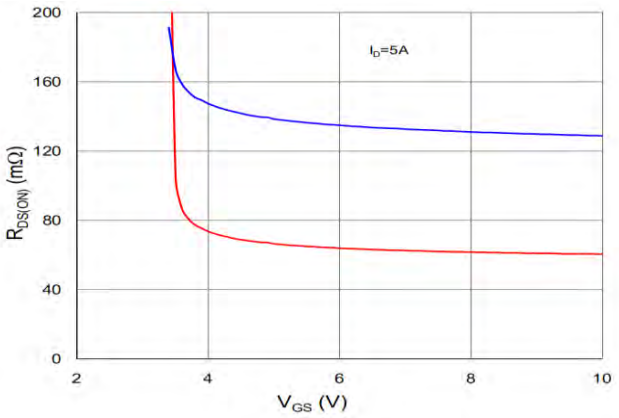


Figure7. On-Resistance vs. Gate-Source Voltage

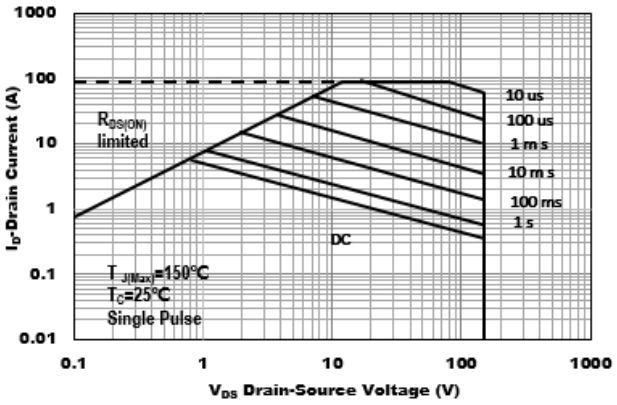


Figure8. Safe Operation Area

Figure A: Gate Charge Test Circuit & Waveforms

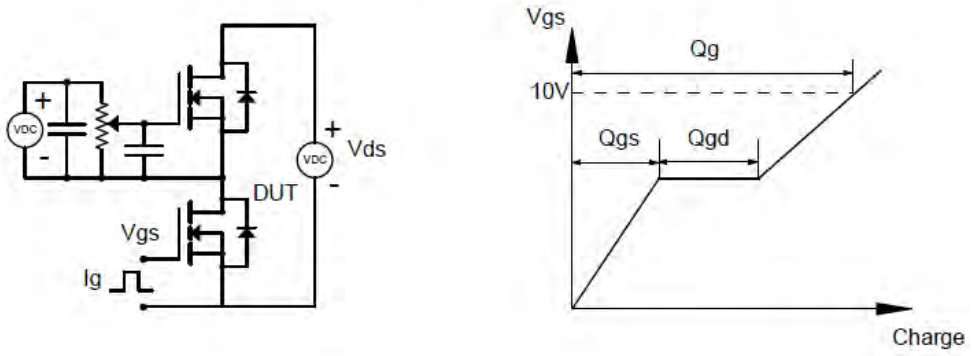


Figure B: Resistive Switching Test Circuit & Waveforms

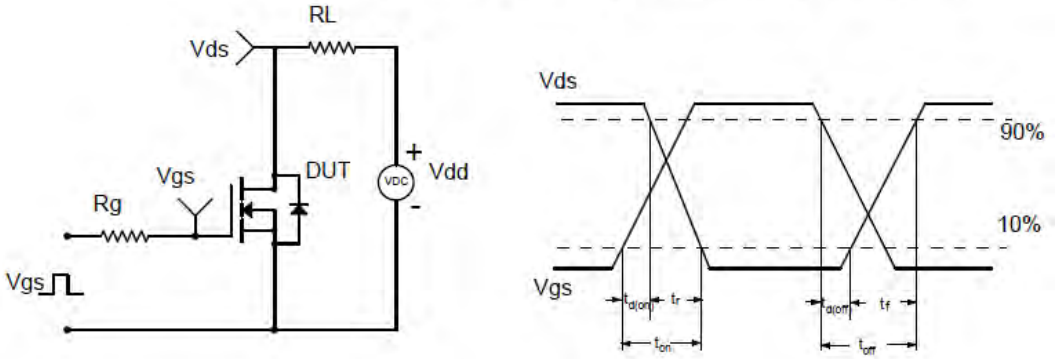


Figure C: Unclamped Inductive Switching (UIS) Test

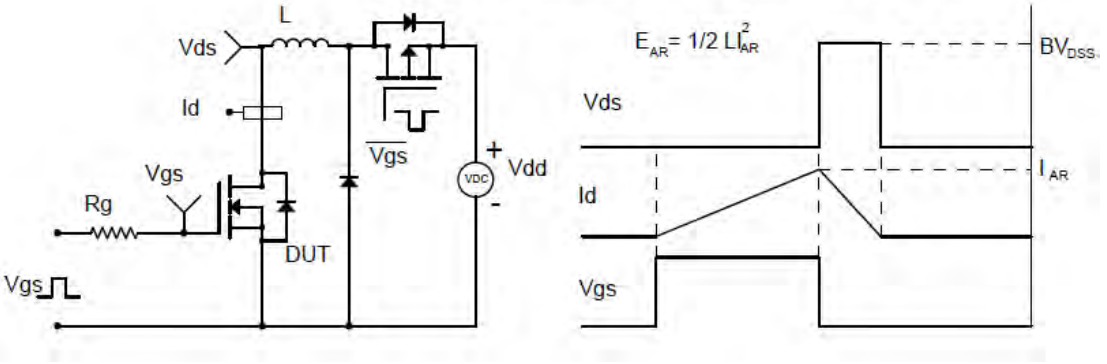
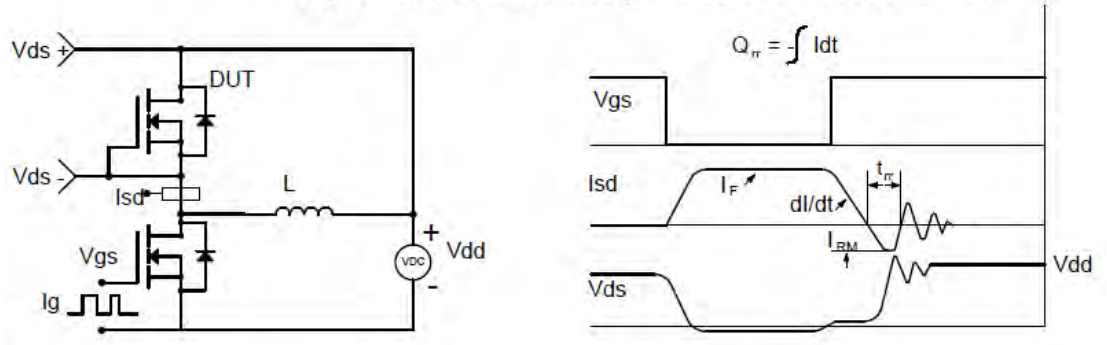
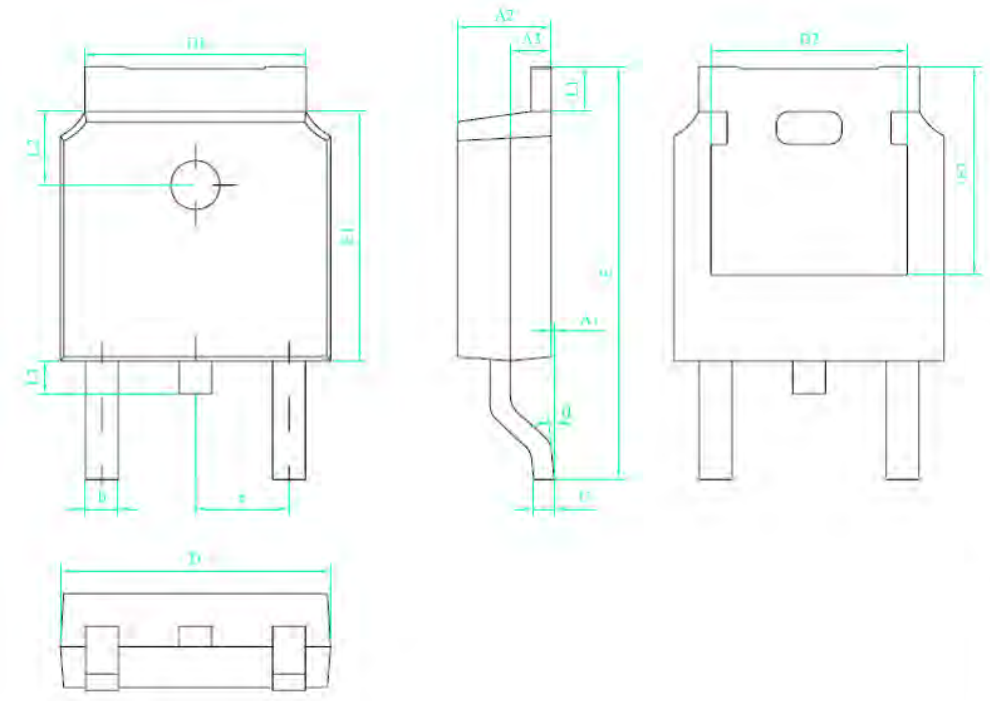


Figure D: Diode Recovery Test Circuit & Waveforms



■TO-252 Package information



符号	尺寸		
	min	nom	max
A1	0	----	0.10
A2	2.20	2.30	2.40
A3	0.90	1.00	1.10
b	0.75	----	0.85
c	0.50	----	0.60
D	6.50	6.60	6.70
D1	5.30	5.40	5.50
D2	4.70	4.80	4.90
E	9.90	10.10	10.30
E1	6.00	6.10	6.20
E2	5.20	5.30	5.40
e	2.20	2.286	2.40
L1	0.90	----	1.25
L2	1.70	1.80	1.90
L3	0.60	0.80	1.00
θ	0°	----	8°

技术要求：
1. 树脂体不应有崩裂、缺损等缺陷；
2. 树脂上下部X、Y方向偏差不超过0.20；
3. 胶体两端留废胶总和宽度不超过0.50；
4. 所有单位为mm；

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