

General Description

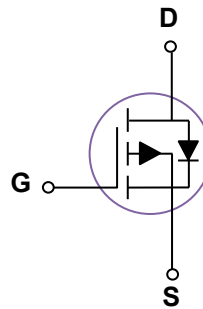
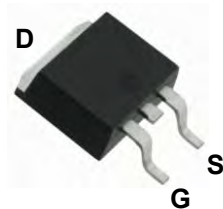
These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

V_{DS}	-40V
I_D (at $V_{GS}=-10V$)	-20A
$R_{DS(ON)}$ (at $V_{GS}=-10V$)	45mΩ(Max)
$R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	65mΩ(Max)

100% UIS TESTED!
100% ΔV_{ds} TESTED!

TO252



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units	
Drain-Source Voltage	V_{DS}	-40	V	
Gate-Source Voltage	V_{GS}	± 20	V	
Drain Current-Continuous	TC=25°C	I_D	-20	A
	TC=100°C	I_D	-12	A
Drain Current – Pulsed	I_{DM}	-80	A	
Maximum Power Dissipation	P_D	33	W	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C	

Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance junction-case	$R_{\theta jc}$		3.6	°C /W
Thermal Resistance junction-to-Ambient	$R_{\theta JA}$		62	°C /W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-40			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-40V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.0	-1.6	-2.5	V
R _{DS(on)}	Drain-Source On-State Resistance	V _{GS} =-10V, I _D =-10A		37	45	mΩ
		V _{GS} =-4.5V, I _D =-5A		57	65	mΩ
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{DS} =-25V, V _{GS} =0V, F=1.0MHz		828		pF
C _{oss}	Output Capacitance			68		pF
C _{rss}	Reverse Transfer Capacitance			50		pF
SWITCHING PARAMETERS						
t _{d(on)}	Turn-on Delay Time	V _{DS} =-20V, I _D =-1A, V _{GS} =-10V, R _G =6Ω		12		nS
t _r	Turn-on Rise Time			13		nS
t _{d(off)}	Turn-Off Delay Time			47		nS
t _f	Turn-Off Fall Time			20		nS
Q _g	Total Gate Charge	V _{DS} =-20V, I _D =-5A, V _{GS} =-4.5V		7.6		nC
Q _{gs}	Gate-Source Charge			2.3		nC
Q _{gd}	Gate-Drain Charge			3.1		nC
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _{SD} =-1A		0.72	1.4	V

Note:

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width ≅ 300us , duty cycle ≅ 2%.
3. Essentially independent of operating temperature.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

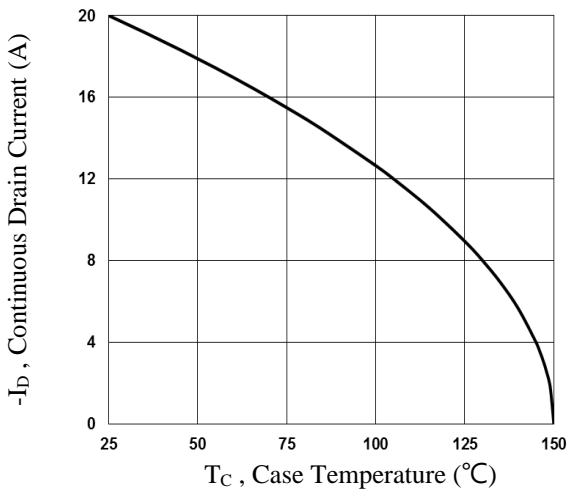


Fig.1 Continuous Drain Current vs. T_C

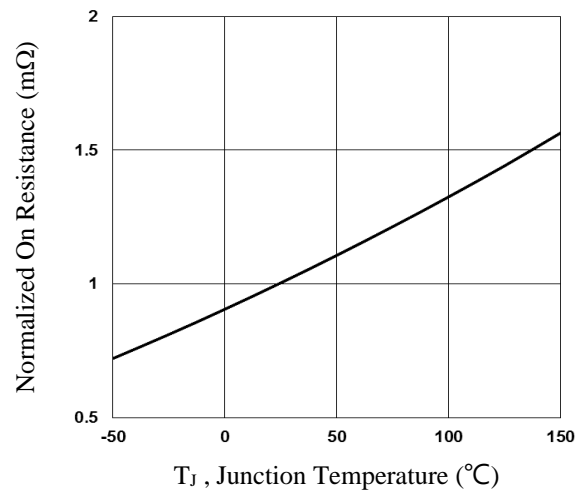


Fig.2 Normalized $R_{DS(on)}$ vs. T_J

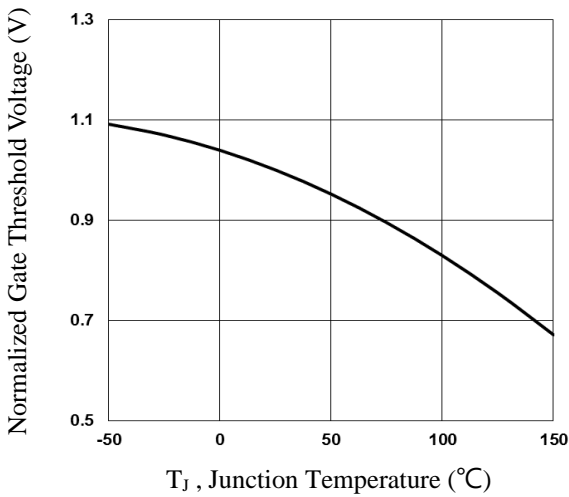


Fig.3 Normalized V_{th} vs. T_J

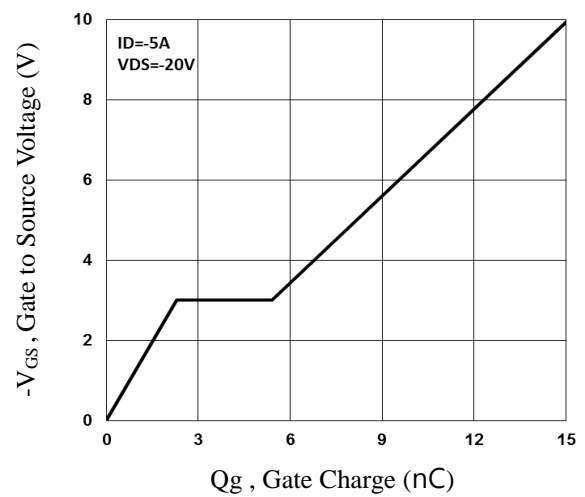


Fig.4 Gate Charge Waveform

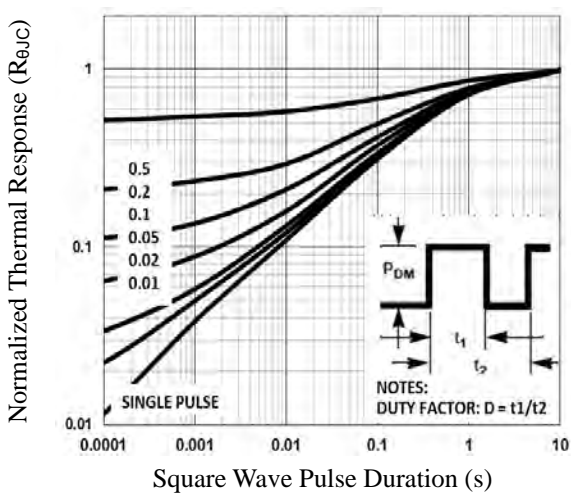


Fig.5 Normalized Transient Impedance

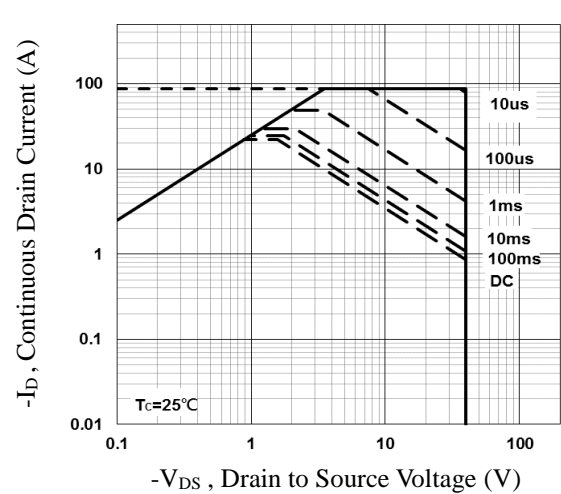


Fig.6 Maximum Safe Operation Area

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

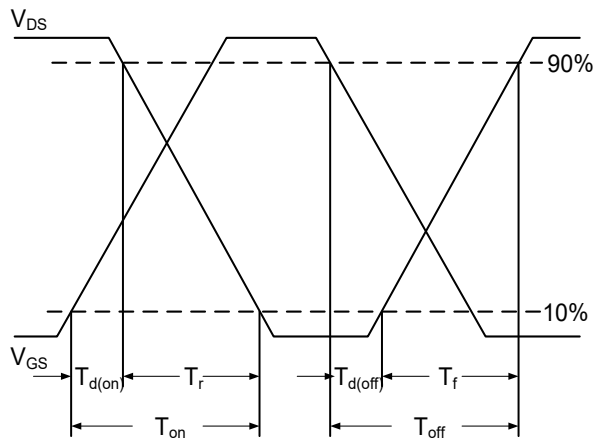


Fig.7 Switching Time Waveform

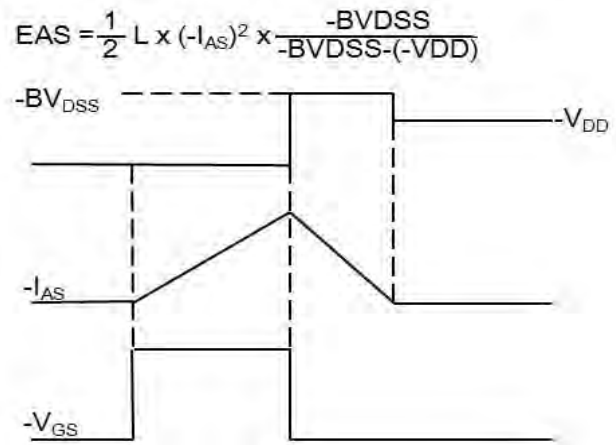
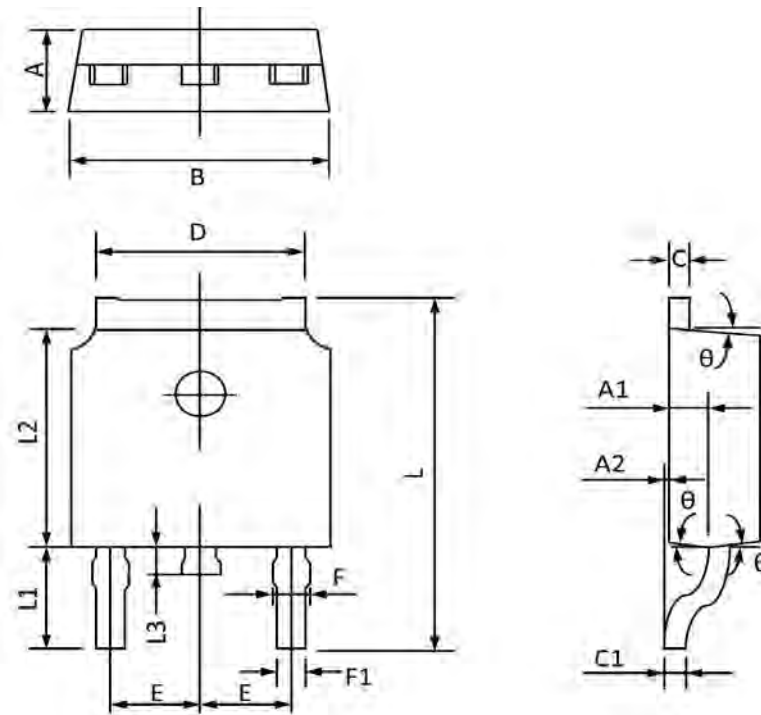


Fig.8 EAS Waveform

TO252 PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.20	2.40	0.087	0.094
A1	0.91	1.11	0.036	0.044
A2	0.00	0.15	0.000	0.006
B	6.50	6.70	0.256	0.264
C	0.46	0.580	0.018	0.230
C1	0.46	0.580	0.018	0.030
D	5.10	5.46	0.201	0.215
E	2.186	2.386	0.086	0.094
F	0.74	0.94	0.029	0.037
F1	0.660	0.860	0.026	0.034
L	9.80	10.40	0.386	0.409
L1	2.9REF		0.114REF	
L2	6.00	6.20	0.236	0.244
L3	0.60	1.00	0.024	0.039
θ	3°	9°	3°	9°